REMARKS/ARGUMENTS

Reconsideration of the present application is politely requested. Claims 1-20 remain active in the case. In order to more particularly point out and distinctly claim that which the applicants regard as their invention, claim 1 has been amended. No new matter in introduced by this amendment.

1. Rejection of claim 1:

Claim 1 was rejected under 35 U.S.C. 103(a), for reasons of record that can be found on pages 3-4 in the Office action identified above, which is Part of Paper No./Mail Date 0705. Claim 1 was rejected by the Examiner under 103 as being unpatentable over Yamagishi et al. (US 6,809,790) in view of Wilson et al. (Handbook of Multilevel Metallization for Integrated Circuits – Materials, Technology, and Applications; William Andrews Publishing/ Noyes; 1993; ISBN 0-8155-1340-2).

The applicants believe that the claimed invention in claim 1 as a whole is allowable because of the following reasons. First of all, none of the cited prior art references teaches "depositing a *molybdenum-containing metal layer* on a *glass substrate*" and then "*etching said molybdenum-containing metal layer to form said gate and word line array pattern having substantially oblique sidewalls*", as required by the amended claim 1. Yamagishi et al. teaches a method for fabricating a matrix substrate and reflection type liquid crystal display device thereof. Please refer to FIGS. 1A, 2A, 4A and 7, and also the related description such as col. 8, lines 4-20, it is respectfully noted that Yamagishi et al. teaches that the *gate electrodes 304 are made of polysilicon* and are formed on a *semiconductor substrate 301, on which a plurality of ion wells and source/drain are implanted*. The "glass substrate", in col. 16, line 7 of Yamagishi, used by the Examiner against claim 1 is not the "substrate" on which the gate and array are resting and formed.

Secondly, in the Office action identified above, the Examiner has indicated that Yamagishi et al. discloses, in col. 8, lines 23-25, forming a patterned photo resist defining a gate 304 (FIG. 1A). However, the applicants found that this is not the case. In effect, the

patterned photo resist cited in col. 8, lines 23-25 of Yamagishi et al. is obviously formed *on the semiconductor substrate 301* and is used as an *implant mask for source/drain implantation*, rather than an *etching mask on the molybdenum-containing metal layer for defining gate and word line array pattern* as required by the amended claim 1. It is respectfully noted that the "*molybdenum-containing metal layer (col. 9, line 41; the metal layer 106)*"used by the Examiner against claim 1 *is a pixel electrode layer 312 is deposited over the entire surface of the substrate 301* (FIG. 1D).

The Examiner has also indicated that Yamagishi et al. discloses depositing a molybdenum-containing metal layer (col. 9, line 41); using a patterned photo resist as a mask (col. 8, line 43); etching (col. 8, line 9) molybdenum-containing metal layer to form gate 304 (FIG. 1A). The applicants submit that *the metal layer 106* (col. 9, line 41; FIG. 1B) used by the Examiner against claim 1 *is merely used to form a rigid tungsten region at the base of the separation regions between the pixels* (col. 9, lines 10-12), *and has nothing to do with the formation of the underlying polysilicon gate electrode 304*. Yamagishi et al. never suggests or implies using the metal layer 106 as a gate material. Again, it is respectfully noted that the *gate electrodes 304 are made of polysilicon and are formed on a semiconductor substrate 301.*

Further, the Examiner has also indicated that Wilson et al. teaches metal lines having tapered sidewalls. However, Wilson et al. teaches nothing about *molybdenum-containing metal layer and etching the molybdenum-containing metal layer on a glass substrate.* Wilson et al. provides a solution to solve step coverage, however, it contains no solution to solve the Mura defect that occurs during the etching of the molybdenum-containing metal layer (metal gate material), which the claimed invention as an aim for. There is nothing that the applicants can find in Wilson et al. that would serve as a motivation to modify Yamagishi reference.

"In determining the differences between the prior art and the claims, the question under 35 U.S.C. 103 is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious." Stratoflex, Inc.

v. Aeroquip Corp., 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); Schenck v. Nortron Corp., 713 F.2d 782, 218 USPQ 698 (Fed. Cir. 1983).

"In determining whether the invention as a whole would have been obvious under 35 U.S.C. 103, we must first delineate the invention as a whole. In delineating the invention as a whole, we look not only to the subject matter which is literally recited in the claim in question but also to those properties of the subject matter which are inherent in the subject matter and are disclosed in the specification. Just as we look to a chemical and its properties when we examine the obviousness of a composition of matter claim, it is this invention as a whole, and not some part of it, which must be obvious under 35 U.S.C. 103." In re Antonie, 559 F.2d 618, 620, 195 USPQ 6,8 (CCPA 1977).

It is respectfully suggested that, in light of the above, none of the cited references, alone or in combination, teaches or makes obvious all of the limitations of the amended claim 1. Reconsideration of claim 1 is therefore politely requested. As Claims 2-12 are dependent upon claim 1, they should be allowable if claim 1 is allowed. Reconsideration of claims 2-12 is therefore politely requested.

2. Rejection of claim 5:

Claim 5 was rejected because of Yamagishi et al. (US 6,809,790) and Wilson et al., in view of Celii et al. (US 2003/0143853).

The Examiner has stated that Celii et al. in tables 3-5 teaches controlling gas flow rates. The applicants believe that this rejection is an error because the parameters cited in tables 3-5 are employed in a *chemical vapor deposition (CVD) process*, but not in an *etching process*. Reconsideration of claim 5 is therefore politely requested.

3. Rejections of claims 6 and 19:

Claims 6 and 19 were rejected because of Yamagishi et al. (US 6,809,790) and Wilson et al.

The Examiner has stated that Yamagishi discloses a multiple metal layers including: aluminum electrodes (col. 8, lines 34-36), aluminum alloy layers (col. 9, lines 3-4), a shielding layer (FIG. 1A: 350-Ti, 105-TiN, 106-W), and a base layer (col. 9, lines 11-12).

However, none of these metals taught by Yamagishi is employed as a gate material. Yamagishi teaches away etching a *molybdenum-containing dual metal layer on a glass substrate into a gate*. Reconsideration of claims 6 and 19 is politely requested.

4. Rejections of claims 7 and 20:

Claims 7 and 20 were rejected because of Yamagishi et al. (US 6,809,790) and Wilson et al., in view of Kim et al. (USAN 10/327,084).

The Examiner has stated that Kim teaches use of a three metal layer, Cr/AlNd/Mo, for source, drain, and data line electrodes (FIG. 8, 141, 143, and 145), as in claims 7 and 20. The Examiner alleged that some of the metals and alloys thereof are the same as the claimed metals and the disclosed invention would have the same capability as the limitation claimed. The applicants respectfully disagree with. Kim teaches use of a three metal layer, Cr/AlNd/Mo, for source, drain and data line electrodes, however, Kim does not teach use of Mo/AlNd, MoW/AlNd, or MoW/Al for gate materials. Further, the applicants submit that Kim teaches away the dual-metal layer is Mo/AlNd, MoW/AlNd, or MoW/Al, wherein Mo and MoW are top layers, while AlNd and Al are bottom layers, as required by the amended claims 7 and 20.

5. Rejection of claim 13:

Claim 13 was rejected under 35 U.S.C. 103(a), for reasons of record that can be found on page 5 in the Office action identified above, which is Part of Paper No./Mail Date 0705. Claim 13 was rejected by the Examiner under 103 because of Yamagishi et al. in view of Wilson et al.

The applicants believe that the claim 13 is allowable because of the following reasons. First, none of the cited prior art references teaches "depositing a *molybdenum-containing metal layer* on a *glass substrate*" and then "*etching said molybdenum-containing metal layer to form said gate and word line array pattern*", as required by claim 13. Yamagishi et al. teaches a method for fabricating a matrix substrate and reflection type liquid crystal display device thereof. Please refer to FIGS. 1A, 2A, 4A and 7, and also the related description such as col. 8, lines 4-20, it is respectfully noted

that Yamagishi et al. teaches that the *gate electrodes 304 are made of polysilicon* and are formed on a *semiconductor substrate 301, on which a plurality of ion wells and source/drain are implanted*. The "glass substrate", in col. 16, line 7 of Yamagishi, used by the Examiner against claim 13 is not the "substrate" on which the gate and array are resting and formed.

Secondly, in the Office action identified above, the Examiner has indicated that Yamagishi et al. discloses, in col. 8, lines 23-24 and line 42, forming a patterned photo resist defining a gate 204 (FIG. 39E). However, the applicants found that this is not the case. In effect, the patterned photo resist cited in col. 8, lines 23-24 of Yamagishi et al. is obviously formed *on the semiconductor substrate 301* and is used as an *implant mask for source/drain implantation*, rather than an *etching mask on the molybdenum-containing metal layer for defining gate and word line array pattern* as required by claim 13. It is respectfully noted that the "*molybdenum-containing metal layer (col. 9, line 41; the metal layer 106)*"used by the Examiner against claim 13 *is a pixel electrode layer 312 is deposited over the entire surface of the substrate 301* (FIG. 1D). Further, numeral number 204 in FIG. 39E is not a gate, but a dielectric layer.

The applicants submit that *the metal layer 106* (col. 9, line 41; FIG. 1B) used by the Examiner against claim 1 *is merely used to form a rigid tungsten region at the base of the separation regions between the pixels* (col. 9, lines 10-12), and has nothing to do with the formation of the underlying polysilicon gate electrode 205 (FIG. 39E). Yamagishi et al. never suggests or implies using the metal layer 106 (col. 9, line 41; FIG. 1B) as a gate material. Again, it is respectfully noted that the *gate electrodes 205 are made of polysilicon and are formed on a semiconductor substrate 301.*

"In determining the differences between the prior art and the claims, the question under 35 U.S.C. 103 is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious." Stratoflex, Inc. v. Aeroquip Corp., 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); Schenck v. Nortron Corp., 713 F.2d 782, 218 USPQ 698 (Fed. Cir. 1983).

"In determining whether the invention as a whole would have been obvious under 35 U.S.C. 103, we must first delineate the invention as a whole. In delineating the invention as a whole, we look not only to the subject matter which is literally recited in the claim in question... but also to those properties of the subject matter which are inherent in the subject matter and are disclosed in the specification. Just as we look to a chemical and its properties when we examine the obviousness of a composition of matter claim, it is this invention as a whole, and not some part of it, which must be obvious under 35 U.S.C. 103." In re Antonie, 559 F.2d 618, 620, 195 USPQ 6,8 (CCPA 1977).

It is respectfully suggested that, in light of the above, none of the cited references, alone or in combination, teaches or makes obvious all of the limitations of the amended claim 13. Reconsideration of claim 13 is therefore politely requested. As Claims 14-20 are dependent upon claim 13, they should be allowable if claim 13 is allowed. Reconsideration of claims 14-20 is therefore politely requested.

Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Sincerely yours,

Winston Hsu Date: 11/13/2006

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)